This SPI Master implementation comprises of a clock divider and spi driver which are connected together to create an SPI Master.

The Clock Divider divides the system clock in order to create an spi\_clk with lower frequency. The clock divider is implemented with reset and decides when to assert / deassert the spi clock based on the value of an internal counter. The clock divider also automatically deasserts the spi\_clk when the spi transaction is complete.

MOSI and MISO were latched together via a direct sequential assignment on the negative edge of SCLK.

1 SPI Transaction in modelsim (All Signals)

A screenshot of a computer

Description automatically generated

3 SPI Transactions in modelsim (All Signals)

A screenshot of a computer

Description automatically generated

1 SPI Transaction in Modelsim (Relevant Signals)

A screenshot of a computer

Description automatically generated

3 SPI Transactions in Modelsim (Relevant Signals):

A screen shot of a computer

Description automatically generated